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(TM.)

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A microprocessor system comprising:

an address generator configured to simultaneously generate a first memory address and a second memory address, wherein the address generator comprises a first adder configured to generate the first memory address, and a second adder configured to generate the second memory address;

a memory system having a first memory tower and a second memory tower; and

an address selector coupled to receive the first memory address and the second memory address and configured to select a first row address for the first memory tower and a second row address for the second memory tower.

2. (Original) The microprocessor system of claim 1, wherein the first row address is equal to a row portion of the first memory address, and the second row address is equal to a row portion of the second memory address.

3. (Original) The microprocessor system of claim 1, wherein the first row address is equal to a row portion of the second memory address, and the second row address is equal to a row portion of the first memory address.

4. (Canceled)

5. (Currently Amended) The microprocessor system of claim 4¹, wherein the first adder adds a first address operand and a second address operand.

6. (Original) The microprocessor system of claim 5, wherein the second adder adds the first address operand, the second address operand, and a carry bit.

7. (Original) The microprocessor of claim 5, wherein the second adder adds a portion of the first address operand, a portion of the second address operand, and a carry bit.